Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A frequency divider dividing an original clock into a target clock, the frequency of the target clock being equal to the frequency of the original clock divided by M, M being a positive odd integer equal to or greater than 3 ~~with a frequency factor M being a positive odd number~~, the frequency divider comprising:

a front set circuit comprising:

a first clock generator with a clock input end connected to a trigger clock having a frequency the same as that of the original clock and a trigger phase; and

a first logic gate with a first input end connected to an output end of the first clock generator, and a second input end connected to a signal input end of the first clock generator;

a middle set circuit comprising:

a second clock generator with a clock input end connected to the trigger clock; and

(M-3)/2 serially connected first sets of clock generators with a clock input end of each first set of clock generators connected to the trigger clock, a signal input end of the ~~immediately previous~~ first clock generator within the (M-3)/2 first sets of clock generators connected to an output end of the first logic gate in the front set circuit, and an output end of the last clock generator within the (M-3)/2 first sets of clock generators connected to a signal input end of the second clock generator in the middle set circuit; and

a rear set circuit comprising:

a third clock generator with a clock input end connected to the trigger clock, and a signal input end connected to an output end of the second clock generator in the

middle set circuit; and

a second logic gate with a first input end connected to an output end of the third clock generator in the rear set circuit, a second input end connected to the output end of the second clock generator in the middle set circuit, and an output end for outputting the target clock.

Claim 2 (previously presented): The frequency divider of claim 1, wherein the first clock generator in the front set circuit, the second clock generator in the middle set circuit, and the (M-3)/2 first sets of clock generators are rising-edge-triggered clock generators, and the third clock generator in the rear set of circuit is a falling-edge-triggered clock generator.

Claim 3 (previously presented): The frequency divider of claim 1, wherein the first clock generator in the front set circuit, the second clock generator in the middle set circuit, and the (M-3)/2 first sets of clock generators are falling-edge-triggered clock generators, and the third clock generator in the rear set of circuit is a rising-edge-triggered clock generator.

Claim 4 (currently amended): The frequency divider of claim 1, wherein the trigger phase is 0 degrees, ~~which means~~ and the trigger clock is ~~the same as~~ identical to the original clock.

Claim 5 (previously presented): The frequency divider of claim 4, wherein the first clock generator in the front set circuit, the second clock generator in the middle set circuit, and the third clock generator in the rear set of circuit are initially-set-low clock generators, and the (M-3)/2 first sets of clock generators are initially-set-high clock generators.

Claim 6 (original): The frequency divider of claim 1, wherein the first logic gate is a NOR gate, and the second logic gate is an OR gate.

Claim 7 (currently amended): A non-integer frequency divider for dividing an original clock to form a target clock, the frequency of the target clock being equal to the frequency of the original clock divided by (2n+1)/2, n being a positive integer equal to or greater than 1 ~~such that the frequency of the original clock is the frequency of the target clock divided n.5 times~~, the non-integer frequency divider comprising:

a phase shifter for generating a first clock and a second clock according to the original clock;

a first dividing circuit receiving the first clock and generating a first target clock in cooperation with a first front set circuit, a first middle set circuit and a first rear set circuit connected serially in sequence inside, wherein the first front set circuit comprises a first clock generator and a first logic gate, the first middle set circuit comprises a second clock generator, k_1 serially connected first sets of clock generators in which $k_1 \geq 0$, and $n-k_1-1$ serially connected second sets of clock generators in which $n-k_1-1 \geq 0$, the k_1 serially connected first sets of clock generators being initially set to different values than the $n-k_1-1$ serially connected second sets of clock generators ~~and in which k_1 is determined according to n and a trigger phase of the first clock~~, and the first rear set circuit comprises a third clock generator and a second logic gate;

a second dividing circuit receiving the second clock and generating a second target clock in cooperation with a second front set circuit, a second middle set circuit and a second rear set circuit connected serially in sequence inside, wherein the second front set circuit comprises a fourth clock generator and a third logic gate, the second middle set circuit comprises a fifth clock generator, k_2 serially connected third sets of clock generators in which $k_2 \geq 0$, and $n-k_2-1$ serially connected fourth sets of clock generators in which $n-k_2-1 \geq 0$, the k_2 serially

connected third sets of clock generators being initially set to different values than the n-k_2-1 serially connected fourth sets of clock generators ~~and in which k_2 is determined according to n and a trigger phase of the second clock~~, and the second rear set circuit comprises a sixth clock generator and a fourth logic gate; and

a synthesizing circuit outputting the target clock according to the first target clock and the second target clock.

Claim 8 (original): The non-integer frequency divider of claim 7, wherein the first clock generator, the second clock generator, the k_1 serially connected first sets of clock generators, and the n-k_1-1 serially connected second sets of clock generators are rising-edge-triggered clock generators, and the third clock generator is a falling-edge-triggered clock generator.

Claim 9 (original): The non-integer frequency divider of claim 7, wherein the first clock generator, the second clock generator, the k_1 serially connected first sets of clock generators, and the n-k_1-1 serially connected second sets of clock generators are falling-edge-triggered clock generators, and the third clock generator is a rising-edge-triggered clock generator.

Claim 10 (original): The non-integer frequency divider of claim 7, wherein the fourth clock generator, the fifth clock generator, the k_2 serially connected third sets of clock generators, and the n-k_2-1 serially connected fourth sets of clock generators are rising-edge-triggered clock generators, and the sixth clock generator is a falling-edge-triggered clock generator.

Claim 11 (original): The non-integer frequency divider of claim 7, wherein the fourth clock generator, the fifth clock generator, the k_2 serially connected third sets of clock generators, and the n-k_2-1 serially connected fourth sets of clock generators are

falling-edge-triggered clock generators, and the sixth clock generator is a rising-edge-triggered clock generator.

Claim 12 (currently amended): The non-integer frequency divider of claim 7, wherein a clock input end of the second clock generator in the first middle set circuit is connected to the first clock, a clock input end of each of the k_1 serially connected first sets of clock generators is connected to the first clock, an output end of the last clock generator in the k_1 first sets of clock generators is connected to a signal input end of the second clock generator, a clock input end of each of the $n-k_1-1$ serially connected second sets of clock generators is connected to the first clock, a signal input end of the ~~immediately previous one~~ first clock generator of the second sets of clock generators is connected to an output end of the first logic gate, and an output end of the last ~~one~~ clock generator of the second sets of clock generators is connected to a signal input end of the ~~most previous one~~ first clock generator of the k_1 first sets of clock generators.

Claim 13 (original): The non-integer frequency divider of claim 12, wherein the second clock generator and the k_1 serially connected first sets of clock generators are initially-set-low clock generators, and the $n-k_1-1$ serially connected second sets of clock generators are initially-set-high clock generators.

Claim 14 (currently amended): The non-integer frequency divider of claim 7, wherein a clock input end of the fifth clock generator in the second middle set circuit is connected to the second clock, a clock input end of each of the k_2 serially connected third sets of clock generators is connected to the second clock, an output end of the last clock generator in the k_2 third sets of clock generators is connected to a signal input end of the fifth clock generator, a clock input end of each of the $n-k_2-1$ serially connected fourth sets of clock generators is connected to the second clock, a signal

input end of the ~~most previous one~~ first clock generator of the fourth sets of clock generators is connected to an output end of the third logic gate, and an output end of the last ~~one~~ clock generator of the fourth sets of clock generators is connected to a signal input end of the ~~immediately previous one~~ first clock generator of the k_2 third sets of clock generators.

Claim 15 (original): The non-integer frequency divider of claim 14, wherein the fifth clock generator and the k_2 serially connected third sets of clock generators are initially-set-low clock generators, and the $n-k_2-1$ serially connected fourth sets of clock generators are initially-set-high clock generators.

Claim 16 (original): The non-integer frequency divider of claim 7, wherein the synthesizing circuit comprises an XOR gate.

Claim 17 (original): The non-integer frequency divider of claim 7, wherein a clock input end of the first clock generator in the first front set circuit is connected to the first clock, the first logic gate is a NOR gate with a first input end connected to an output end of the first clock generator and a second input end connected to a signal input end of the first clock generator, a clock input end of the third clock generator in the first rear set circuit is connected to the first clock, a signal input end of the third clock generator in the first rear set circuit is connected to an output end of the second clock generator in the first middle set circuit, the second logic gate is an OR gate with a first input end connected to an output end of the third clock generator and a second input end connected to an output end of the second clock generator in the first middle set circuit, and the output end generates the first target clock.

Claim 18 (currently amended): The non-integer frequency divider of claim 7, wherein a clock input end of the fourth clock generator in the second front set circuit is

connected to the second clock, the third logic gate is a NOR gate with a first input end connected to an output end of the fourth clock generator and a second input end connected to a signal input end of the fourth clock generator, a clock input end of the sixth clock generator in the second rear set circuit is connected to the second clock, a signal input end of the sixth clock generator in the second rear set circuit is connected to an output end of the fifth clock generator in the second middle set circuit, the fourth logic gate is an OR gate with a first input end connected to an output end of the sixth clock generator and a second input end connected to an output end of the fifth clock generator in the second middle set circuit, and the output end generates the ~~first~~ second target clock.

Claim 19-21 (cancelled).

Claim 22 (new): A frequency divider dividing an original clock into a target clock, the frequency of the target clock being equal to the frequency of the original clock divided by M, M being a positive odd integer equal to or greater than 3, the frequency divider comprising:

a front set circuit comprising:

a first clock generator with a clock input end connected to a trigger clock having a frequency the same as that of the original clock and a trigger phase; and

a first logic gate with a first input end connected to an output end of the first clock generator, and a second input end connected to a signal input end of the first clock generator;

a middle set circuit comprising:

a second clock generator with a clock input end connected to the trigger clock, and a signal input end connected to an output end of the first logic gate in the front set circuit; and

a rear set circuit comprising:

a third clock generator with a clock input end connected to the trigger clock, and a signal input end connected to an output end of the second clock generator in the middle set circuit; and

a second logic gate with a first input end connected to an output end of the third clock generator in the rear set circuit, a second input end connected to the output end of the second clock generator in the middle set circuit, and an output end for outputting the target clock.

Claim 23 (new): The frequency divider of claim 22, wherein the first clock generator in the front set circuit and the second clock generator in the middle set circuit are rising-edge-triggered clock generators, and the third clock generator in the rear set of circuit is a falling-edge-triggered clock generator.

Claim 24 (new): The frequency divider of claim 22, wherein the first clock generator in the front set circuit and the second clock generator in the middle set circuit are falling-edge-triggered clock generators, and the third clock generator in the rear set of circuit is a rising-edge-triggered clock generator.

Claim 25 (new): The frequency divider of claim 22, wherein the trigger phase is 0 degrees, and the trigger clock is identical to the original clock.

Claim 26 (new): The frequency divider of claim 25, wherein the first clock generator in the front set circuit, the second clock generator in the middle set circuit, and the third clock generator in the rear set of circuit are initially-set-low clock generators.

Claim 27 (new): The frequency divider of claim 22, wherein the first logic gate is a NOR gate, and the second logic gate is an OR gate.

Claim 28 (new): A method for designing a frequency divider to divide an original clock to form a target clock, the method comprising:

phase shifting the original clock to generate a first clock and a second clock according to the original clock, the first clock and the second clock being out of phase with each other and each having the same frequency as the original clock;

dividing the frequency of each of the first clock and the second clock by a factor of M to respectively generate first and second divided clocks, M being a positive odd integer equal to or greater than 3; and

performing an XOR logic operation on the first and second divided clocks to generate the target clock with a frequency that is twice the frequency of the first and second divided clocks.

Claim 29 (new): The method of claim 28, wherein the first and second clocks are 90 degrees out of phase with each other.

Claim 30 (new): The method of claim 29, wherein the first and second divided clocks each have a duty cycle of 50%.